Claim Amendments

Claim 1 (currently amended): An apparatus for storing packets comprising:

a memory for holding packets; and

a mechanism for storing at least one packet in the memory with only one packet boundary indicator associated with it, the storing mechanism includes a memory controller, the memory controller places a packet boundary indicator in the memory after a predetermined number of bits have been stored in the memory, the memory is defined by cache lines and the packets are stored along cache lines in the memory, the memory controller stores bits of data of packets in a cache line in the memory, and an identifier in the cache line of data indicating how many bits in the cache line are valid.

Claims 2-5 (canceled)

Claim 6 (currently amended): An apparatus as described in Claim [[5]] 4 wherein each cache line is 200 bits long.

Claim 7 (original): An apparatus as described in Claim 6 wherein the identifier is 2 bits of the 200 bits of each cache line.

Claim 8 (original): An apparatus as described in Claim 7 wherein the memory controller inserts a packet boundary indicator after 15 cache lines worth of packets have been stored in the memory.

Claim 9 (original): An apparatus as described in Claim 8 wherein the memory controller switches which packets are to be transferred from the memory based on packet boundary indicators with respect to priority of the packets.

Claim 10 (currently amended): A method for storing packets comprising the steps of:

receiving packets at a memory; and

storing with a memory controller at least one packet in the memory with only one packet boundary indicator associated with it, the storing step includes the [[step]] steps of placing with the memory controller a packet boundary indicator in the memory after a predetermined number of bits have been stored in the memory, storing the packets along cache

lines in the memory, and storing bits of data of packets in a cache line in the memory, and an identifier in the cache line of data indicating how many bits in the cache line are valid.

Claim 11-13 (canceled)

Claim 14 (currently amended): A method as described in Claim [[13]] 10 including after the storing step, there is the step of switching packets from the memory based on packet boundary indicators with respect to priority of the packets.